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| STEUBING AND MCGUINNESS & MANARAS LLP 125 NAGOG PARK ACTON, MA 01720 | | | DONAGHUE, LARRY D | |
| | | | ART UNIT | PAPER NUMBER |
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DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/213,613

Applicant(s)

GUPTA ET AL.

Examiner

Larry D. Donaghue

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 February 2005 and 09 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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1. Claims 1-9 are presented for examination. *to 10/10/05*
2. Objection to the drawings is withdrawn.
3. As to the rejection of claims 1-3 and 5-9 as being unpatentable over Kedem, U.S. Patent No. 6,167,485, in view of van der Wal, the rejection has been withdrawn because the Applicants' statement of common ownership is sufficient under 35 U.S.C. 103(c) to exclude Kedem, U.S. Patent No. 6,167,485, as prior art. See the response filed on 09/09/2004 and 02/02/2005 (paper no. 22) at page 8.
4. As to the rejection of claim 4 as being unpatentable over Kedem, U.S. Patent No. 6,167,485, in view of van der Wal, and further in view of Sato, the rejection has been withdrawn because the Applicants' statement of common ownership is sufficient under 35 U.S.C. 103(c) to exclude Kedem, U.S. Patent No. 6,167,485, as prior art. See the response filed on 09/09/2004 and 02/02/2005 at page 8.
5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Symmetrix Model 5500 Product Manual, Rev. G, EMC Corp., pp. 1-236 (Symmetrix Product Manual), in view of Litt, U.S. Patent No. 5,815,651, and further in view of van der Wal, A., "Efficient Interprocessor Communication in a Tightly Coupled Homogenous Multiprocessor System," Proc. of the IEEE Workshop on Future Trends of Distributed Computing Systems, IEEE, pp. 362-368, October 1990.

Regarding claim 1, the Symmetrix Product Manual teaches the invention substantially as claimed by disclosing a system comprising a shared service processor providing a single point of contact for a user interfacing with at least one line processor (pp. 11 and 21-22, particularly Fig. 3 on p. 22 showing the line processors/channel directors and the service processor). The Symmetrix Product Manual teaches that the service processor communicates with the line processors via a serial interface (p. 21, discussion of service processor- service processor communicates with Symmetrix subsystem using RS-232 interface). The fact that the service processor and the Symmetrix subsystem processors communicate implicitly shows that they exchange messages.

The Symmetrix Product Manual therefore does not teach a system wherein: (a) the service processor is in electrical communication with shared memory including mailboxes operable to enable communication between the at least one line processor and the service processor; (b) the service processor is operable to selectively deliver commands to a respective mailbox of a selected one of said at least one line processor; (c) the service processor is selectively operable to issue a system management interrupt to any or all of the at least one line processors, the interrupt signaling to the at least one line processor to access a respective mailbox in the shared memory.

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Litt on the other hand teaches a system in which the a service processor is connected to various controlled processors via a parallel bus as opposed to a serial bus as in the Symmetrix Product Manual (col. 4 lines 20-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of the Symmetrix Product Manual to directly couple the service processor to the line processors using a parallel bus based on Litt's teaching that a parallel data path/bus is an alternative to a serial data bus as in the Symmetrix Product Manual (col. 4 lines 20-28).

The combination of the Symmetrix Product Manual in view of Litt does not teach a system wherein:

(a) the service processor is in electrical communication with shared memory including mailboxes operable to enable communication between the at least one line processor and the service processor; (b) the service processor is operable to selectively deliver commands to a respective mailbox of a selected one of said at least one line processor; (c) the service processor is selectively operable to issue a system management interrupt to any or all of the at least one line processors, the interrupt signaling to the at least one line processor to access a respective mailbox in the shared memory.

van der Wal on the other hand teaches a multiprocessor system in which processors connected on a bus communicate using mailboxes and interrupts (p. 362 second complete paragraph in col. 2). van der Wal therefore teaches a system wherein a processor is in electrical communication with shared memory including mailboxes operable to enable communication between the processors (p. 362 second complete paragraph in col. 2). van der Wal also teaches a system in which one processor is able to selectively deliver messages/commands to a respective mailbox of a selected one of the other processors (p. 362 second complete paragraph in col. 2). van der Wal also the "sending" processor is selectively operable to issue a system management interrupt to any or all of the at least one "receiving" processors, the interrupt signaling to the at least one "receiving" processor to access a respective mailbox in the shared memory (p. 362 second complete paragraph in col. 2). van der Wal therefore teaches a mailbox communication scheme but does not teach its use in the particular context of line and service processors.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine van der Wal's communication scheme using shared memory mailboxes and interrupts with the system of the combination of the Symmetrix Product Manual in view of Litt because a person of ordinary skill in the art would clearly recognize that some interprocessor communication scheme must be selected to implement the system of the combination of the Symmetrix Product Manual in view of Litt. Otherwise, the system could not operate. In this context, of a bus based multiprocessor system as in the combination, a person of ordinary skill in the art would recognize that reducing bus contention caused by polling is an important consideration (van der Wal p. 362 second complete paragraph) and would therefore choose the mailbox scheme using global interrupts described by van der Wal (p. 362 second complete paragraph lines 11-16) because on van der Wal's explicit teaching that most multiprocessor systems use some form of this communication scheme.

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As to claim 2, the combination of the Symmetrix Product Manual in view of Litt and further in view of van der Wal as applied to claim 1 above teaches these features.

Official notice is hereby taken of the fact that an acknowledgement to a message is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the line processor of the combination of the Symmetrix Product Manual in view of Litt and further in view of van der Wal acknowledge a message sent by the command, and then delivers an appropriate response to a mailbox (p. 362).

As to claim 3, the combination of the Symmetrix Product Manual in view of Litt and further in view of van der Wal teaches a system wherein the line processor is operable to assert its system management interrupt line to the service processor after

delivering the appropriate response to the mailbox since van der Wal teaches that all processors can communicate with each other (p. 362).

As to claims 6-8, they are method claims corresponding to apparatus claims 1-3, respectively. Since they do not teach or define above the information in the corresponding apparatus claims, they are rejected under the same basis.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Symmetrix Product Manual in view of Litt, and further in view of van der Wal, as applied to claim 1 above, and further in view of Sato et al.

Regarding claim 4, the combination of the Symmetrix Product Manual in view of Litt and further in view of van der Wal teaches the invention substantially as claimed. See the rejection of claim 1 above. The combination does not teach the additional feature of claim 4.

Sato on the other hand teaches a service processor electrically coupled to a nonvolatile memory/disk drive (Col. 1 lines 17-21). The disk drive stores operating programs for embedded processors/channel controllers. The service processor loads these operating programs into memory when the system powers on (Col. 1 lines 17-26). These operating programs are initialization and/or boot information. Upon considering Sato's teachings, a person of ordinary skill in the art at the time the invention was made would have recognized that Sato's teaching is merely a specific example of the general principle of having a service processor configure a system by loading the executable code for an embedded processor at power up.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Sato's teaching with the system of the combination of the Symmetrix Product Manual in view of Litt and further in view of van der Wal by attaching a disk drive to the Symmetrix Product Manual's service processor and then having the Symmetrix Product Manual's service processor load executable programs from the disk drive into the memories of the host and disk adapter processors at power up. The Symmetrix Product Manual teaches that the service processor configures the components of the storage system (p. 21 downloads the Symmetrix configuration).

Based on this teaching, a person of ordinary skill in the art at the time the invention was made would have made

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the combination because storing the host and disk adapter programs on the service processor's disk drive rather than in ROM co-located with the individual processors would make software upgrades easier.

As to the service processor, Sato does not explicitly teach that the service processor boots from its attached disk drive. However, official notice is hereby taken of the fact that processors with attached disk drives commonly boot from programs stored on the attached disk. It would therefore have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of which official notice is taken with the system of the combination of the Symmetrix Product Manual in view of Litt and further in view of van der Wal and further in view of Sato by having the nonvolatile memory attached to the service processor store initialization and/or boot information for the service processor. This combination would have been obvious because storing the service processor boot and/or initialization information on the attached disk drive makes upgrades to the service processor software easier.

6. Applicant's arguments filed 02/05/2005 and 09/09/2004 have been fully considered but they are not persuasive.

Applicant argues First of all, Litt is combined with the Symmetrix Product Manual for its disclosure of a parallel bus. The Office Action replaces the serial bus of the Symmetrix Product Manual with the parallel bus of Litt to teach, apparently, the claimed "interfacing". The Applicant previously argued that Litt is irrelevant, because the form of interface is not claimed, and therefore there is no need to present prior art teaching a parallel bus. The argument stands. The Office Action further points to the specification regarding the interfacing. It is well settled, however, that claims are not limited to the embodiments presented as implementation examples in the specification.

RESPONSE

Examiner agrees claims are not limited to the embodiments presented as implementation examples in the specification.

Finally, the Applicant argued previously that the motivation to combine van der Wal with the Symmetrix Product Manual and Litt relies upon impermissible hindsight. The Office Action contends that the obviousness rejection is proper because "all assertions of the Examiner made in the rejection have been supported by knowledge gleaned from the references". The Applicant disagrees.

The Applicant was faced with an environment wherein a shared service processor that provides a single point of contact for a user is interfaced with line processors. Van der Wal is concerned with efficient implementation of parallel processing in a multiprocessor environment (p. 362 2nd full paragraph). As previously set forth, many different interprocessor communication schemes could have been chosen by the Applicant in order to reduce bus contention in the target environment. Why would van der Wal's messaging system, as opposed to any other scheme, be selected? Van der Wal makes no such suggestion. The combination is therefore made in light of the Applicant's disclosure regarding the claimed shared service processor environment. And that is impermissible.

RESPONSE

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Van der Wal makes numerous statements to the benefits for adapting multi-processor system sto this communication system;

Avoids bus contention (abstract), the problem of bus contention is solved by a distributed interrupt mechanism using hardware communication registers and distributed computer system that is both modular and flexible and at the same time has a high performance.

Claim 4 was rejected over the combination of the Symmetrix Product Manual in view of Litt and further in view of van der Wal and further in view of Sato. As previously argued, claim 4 depends from claim 1. The addition of Sato to the Symmetrix Product Manual, Litt, and van der Wal fails to solve the deficiencies of the combination as previously described. Thus the applicant asserts that claim 4 is allowable for the reasons set forth with regard to claims 1- 3 and 6 - 8.

RESPONSE

See response above.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larry D. Donaghue whose telephone number is 571-272-3962. The examiner can normally be reached on M-F 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LARRY D. DONAGHUE
PRIMARY EXAMINER

